



US 20030086515A1

(19) United States

(12) Patent Application Publication

Trans et al.

(10) Pub. No.: US 2003/0086515 A1

(43) Pub. Date: May 8, 2003

(54) CHANNEL ADAPTIVE EQUALIZATION PRECODING SYSTEM AND METHOD

(76) Inventors: Francois Trans, Los Altos, CA (US); Tho L. Ngoc, Anjou (CA)

Correspondence Address:
FENWICK & WEST LLP
TWO PALO ALTO SQUARE
PALO ALTO, CA 94306 (US)

(21) Appl. No.: 09/970,628

(22) Filed: Oct. 3, 2001

Related U.S. Application Data

(60) Division of application No. 09/847,097, filed on May 1, 2001, which is a division of application No. 09/550,395, filed on Apr. 14, 2000, and which is a continuation-in-part of application No. 09/444,007, filed on Nov. 19, 1999, which is a continuation-in-part of application No. 09/417,528, filed on Oct. 13, 1999, and which is a continuation-in-part of application No. 09/127,383, filed on Jul. 31, 1998, now Pat. No. 6,377,640.

(60) Provisional application No. 60/170,455, filed on Dec. 13, 1999. Provisional application No. 60/104,316, filed on Oct. 13, 1998. Provisional application No. 60/109,340, filed on Nov. 20, 1998. Provisional application No. 60/129,314, filed on Apr. 14, 1999. Provisional application No. 60/089,526, filed on Jun. 15, 1998. Provisional application No. 60/085,605, filed on May 15, 1998. Provisional application No. 60/054,415, filed on Jul. 31, 1997. Provisional application No. 60/054,406, filed on Jul. 31, 1997.

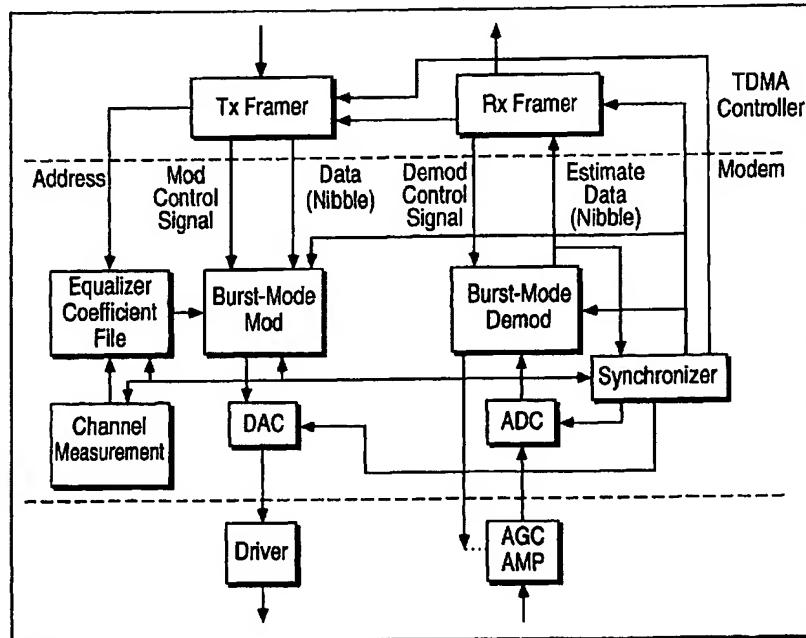
Publication Classification

(51) Int. Cl.⁷ H04L 25/08; H03K 5/01

(52) U.S. Cl. 375/346

ABSTRACT

A system and method for delivering increased speed, security, and intelligence to wireline and wireless systems. The present invention includes a new generation Fast Circuit Switch (packet/circuit) Communication processors and platform which enables a new Internet Exchange Networking Processor Architecture at the edge and core of every communication system, for next generation Web Operating System or Environment (WOE) to operate on with emphasis of a non-local processor or networking processor with remote web computing capabilities.



Burst-Mode Modern Block Diagram

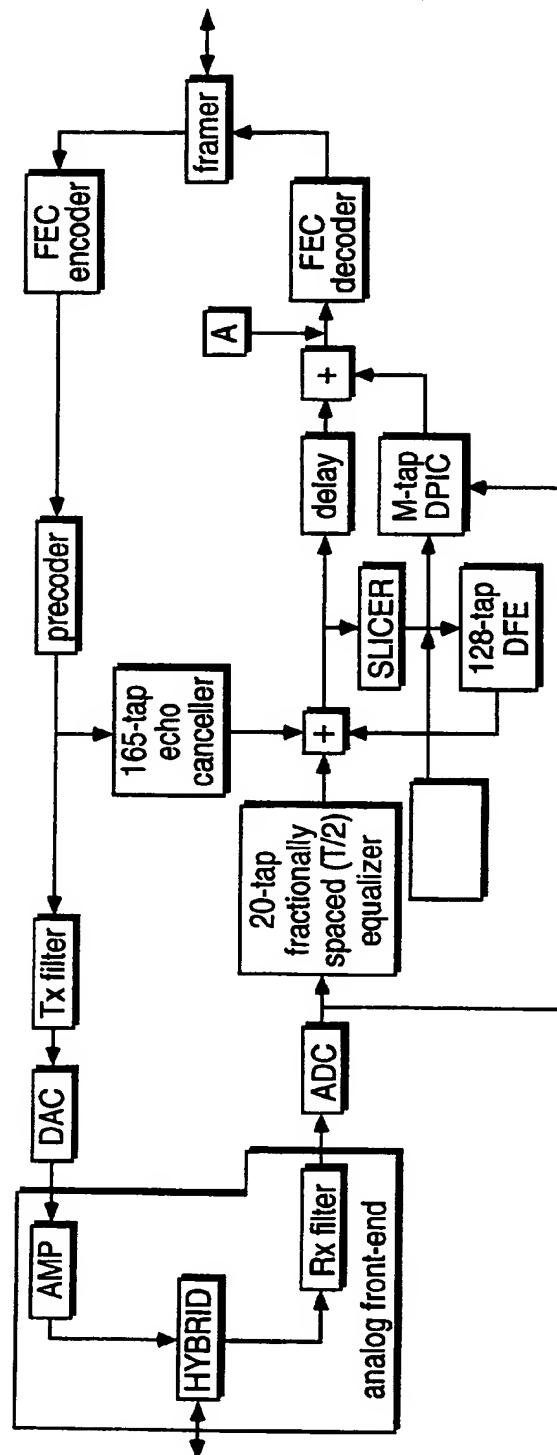


FIG. 31
SNR Measurement Points (A,B) (Proposed Transceiver Structure using DPIC)

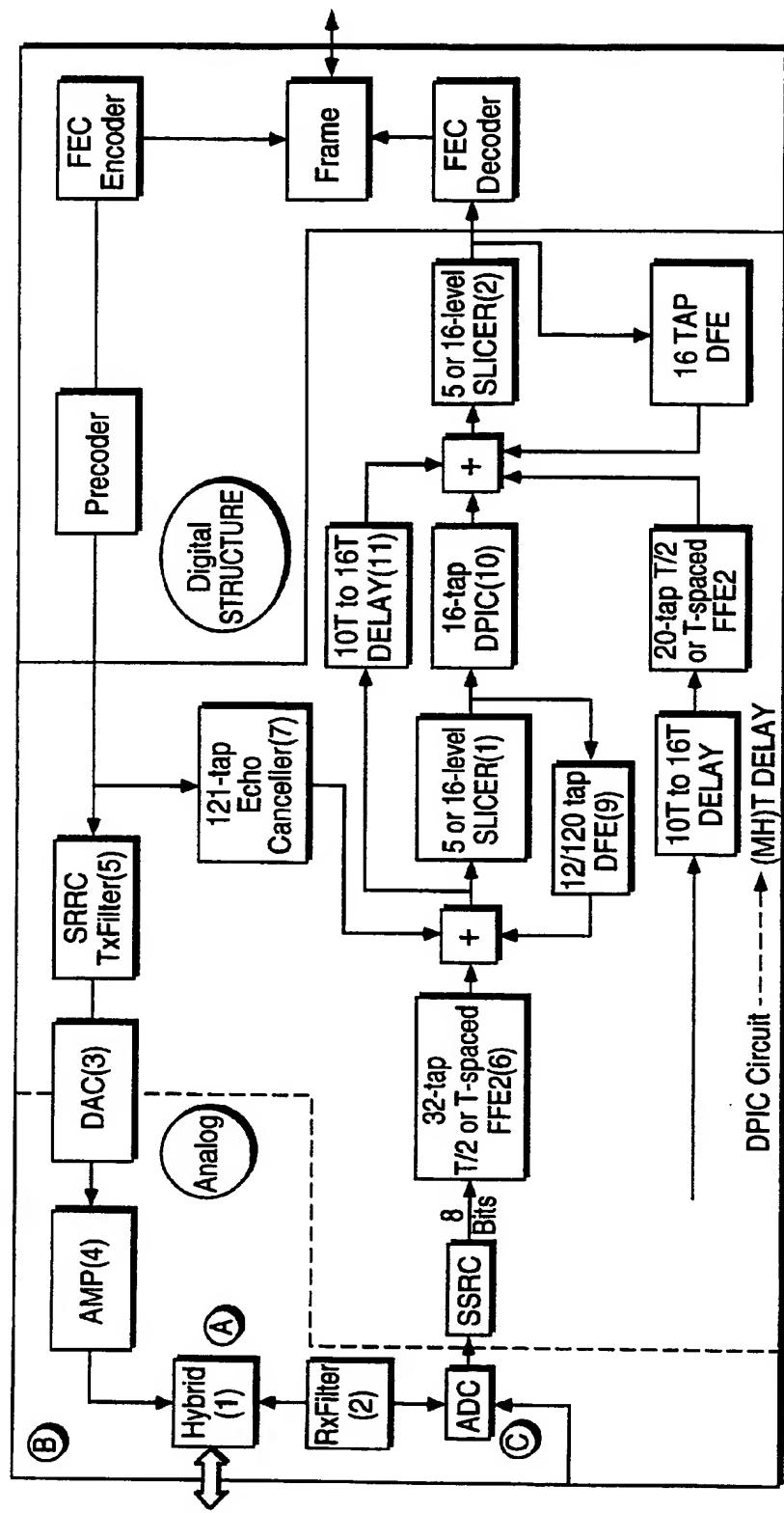


FIG. 32
HDSL2 Front-End (Converter & Sampler & Equalizers)